Wonjong Peter Lee

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Education

University of Illinois Urbana-Champaign Aug. 2021 – May 2027
Bachelor of Science in Computer Engineering *GPA: 3.94/4.0*

- Coursework: Parallel Architecture, Computer Architecture, Parallel Programming, Computer Systems Engineering

Experience

Etched | *Architecture Intern* Aug. 2026 – Dec. 2026

Apple | *CPU Design Intern* May 2026 – Aug. 2026

PASSAT Research Group (Prof. Rakesh Kumar) | *Undergrad Research Assistant* Jan. 2026 – Present

- Designed and implemented RTL for an in-network computing switch targeting Mixture-of-Experts inference workloads; completed synthesis and place-and-route using the ASAP7 PDK.
- Exploring processor-based RTL emulation systems.

Rebellions, Inc. | *Post-Silicon Validation Intern – Live Demo at Hot Chips Symposium* Apr. 2025 – Aug. 2025

- Owned TRACE32-based post-silicon validation flow for core IPs of the REBEL_Quad NPU SoC.
- Built an LLVM/Clang-based transpiler that lowers C firmware to TRACE32 Practice scripts, enabling early validation across 1,000+ workload patterns before CPU, firmware, and DRAM bring-up; the workflow became the preferred early-silicon screening method internally and at a design-house partner.
- Developed a register-programming GUI to accelerate on-silicon debug, failure triage, and chip bring-up.
- Reduced scheduled early bring-up time by ∼30%, contributing to an end-to-end silicon-to-vLLM demo within 30 days of first tapeout arrival and a *Hot Chips 2025* live demo of single-chip Llama 3.3 70B inference.

The Republic of Korea Army | *Sergeant* Sep. 2023 – Mar. 2025

Rivian | *Design Verification Intern* Mar. 2023 – Aug. 2023

- Built Python-based DV infrastructure for NoC simulation with live performance telemetry and a Grafana dashboard for throughput and latency analysis.
- Enhanced UVM testbenches to generate diverse constrained-random traffic profiles, broadening functional coverage of NoC arbitration and routing logic.
- Scaled simulation workloads to 1M+ transactions per DUT port, enabling early detection of design bottlenecks.

University of Illinois | *Undergrad Course Assistant* Jan. 2023 – Aug. 2023

- Held weekly office hours to mentor and support students in ECE 385: Digital Systems Laboratory and ECE 411: Computer Organization and Design.

Projects

RV32IM Out-of-Order Superscalar Processor | *SystemVerilog, VCS, Verdi* Oct. 2025 – Present

- Placed 1st in a course CPU design competition (3-person team).
- Designed and implemented a 2-way superscalar out-of-order RV32IM processor with a GShare branch predictor, non-blocking data cache, checkpoint-based early branch recovery, and next-line prefetching.
- Achieved 60.69× overall performance improvement (PD^4) over baseline and 3.87× over runner-up design; reached ∼1.09 IPC on CoreMark at 648.51 MHz with 0.3 mm^2 total cell area in FreePDK45.

tageBuilder - TAGE Branch Predictor Performance Modeling | *Python* Nov. 2024 – Feb. 2025

- Implemented a parameterized TAGE-like branch predictor model for design-space exploration and tuning.
- Identified a configuration achieving 95% accuracy and 1–3 MPKI on the majority of traces in the CBP-5 dataset.

Unix-like Operating System | *C, QEMU* Apr. 2023 – May 2023

- Collaborated within a team of four to implement a UNIX-like operating system for an x86 uniprocessor system.
- Developed key OS features including a read-only filesystem, multithreading, virtual memory management, interrupt handling, device drivers, and support for system calls such as execute, read, and write.

Skills

HDLs: SystemVerilog, Verilog
Programming & Tools: Python, C/C++, Linux, VCS, Verdi, Innovus, Design Compiler, TRACE32